INSTRUCTION DATA

RFL Industries, Inc., Boonton, New Jersey 07005

Model 66A LD/CD
Lamp Driver and Change Detector

DESCRIPTION

The Model 66A LD/CD is one of the RFL Series 66 TDMS plug-in modules. It monitors the status of each of eight independent points, and it has the capability to drive a single indicating lamp per point for an ON-OFF type of indication. It will cause the lamp to flash at a relatively high rate when the status of the point represented changes from OFF to ON, until acknowledged, after which it burns steadily. Similarly, when the status of the point represented changes from ON to OFF, the lamp flashes at a relatively slower rate, until acknowledged, after which it remains off.

SPECIFICATIONS

Output Drive Current: 160 mA maximum, for each output.

Output Transistor Breakdown Voltage: 40 volts.

Operating Ambient-Temperature Range: −30 to 70°C.

Power Required: 11 to 13Vdc, 10 mA plus lamp current.

Size: One standard one-half-inch module increment in an RFL Model 68 Chassis.

CONNECTIONS

All semiconductors, and especially smaller ones such as small-signal transistors, linear and digital integrated circuits, and microprocessors, are vulnerable to the possibility of damage from static charges. Procedures for minimizing this possibility are outlined in RFL Document 12175A.

All unused input terminals, or unused inputs to integrated circuits, must be returned either to +V or to common.

Indicating lamps, operating with 160 mA or less are connected between a positive voltage source and the open-collector output terminal of each of the lamp-driver circuits. The positive voltage source can be a source different, if desired, from the 12-volt supply used to power the logic circuits, providing the breakdown voltage of the transistor is not exceeded.

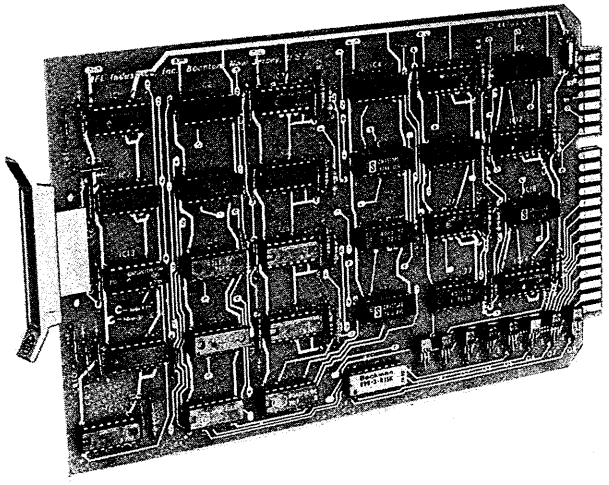

Figure 1. Model 66A LD/CD Lamp Driver and Change Detector.

CIRCUIT DETAILS

This discussion of the circuit is based on Figure 2, in which the circuit of Point 8, at bottom right, has been chosen. Other points are identical. The following abbreviations are used:

$\overline{CO}$	Change Occurred
RGA	Arm General Alarm
$\overline{GA}$	General Alarm
LMP	Lamp

Assume the following initial conditions: IC21B-13 is high, IC21A-1 is high, and IC19B-13 is high. Then, a logic 0 at Terminal 16, STATUS, will cause IC22B-5 to go to a logic 1. Because IC20A-1 is at a logic 0, IC20A-3 must be a logic 1. With a logic 1 on both inputs of IC22B, the output, a logic 0, will cause IC27A-3 to be a logic 0 which keeps Q2 and Lamp 8 in the off state, to indicate an OFF or NO ALARM condition. This state can be acknowledged by momentarily placing a logic 1 at Terminal 19, ARM, which will set IC21A and IC21B. Because these were assumed to be already set, their state will remain unchanged, and so no change of status is indicated at Point 8.

Next, assume that Terminal 16, STATUS, changes from a logic 0 to a 1. This will change IC22B-5 to a logic 0. Moreover, IC21B-13 will change state because of the positive-going transition on its clock input, Pin 11. This, in turn, will cause IC21A to change status because of the positive transition on its reset input at Pin 4. The resulting change at IC21A-1 will take $\overline{CO}$ to a logic 0. IC20D-12 also goes to a logic 1 and so causes IC20D-11 to switch at frequency F_1, and IC20B-4 follows the same frequency. Because IC20A-1 is a logic 1, IC22B-6 will switch at the rate of F_1. This passes through IC22B, IC27A, and Q2 to cause the lamp to flash at frequency F_1. Simultaneously, IC19B-13 takes $\overline{GA}$, GENERAL ALARM, low. This signal may be used to operate an audible alarm.

A momentary logic 1 on Terminal 12, ARM GEN ALARM, will stop the audible alarm, but the lamp will continue to flash. The ON, or ALARM, condition is acknowledged by placing a momentary logic 1 at Terminal 19, ARM, which sets IC21B and IC21A and thus presents a logic 0 at IC20A-1. The resulting logic 1 at IC20A-3 causes IC22B-4 to be high and so holds Lamp 8 steadily illuminated.

Next, assume that a change of state causes Terminal 16 to change from a logic 1 to a logic 0. This will cause IC22B-5 to go to a logic 1. Flip-flop IC21B will not change state, but IC21A will change and will place a logic 0 at IC21A-1 and a logic 1 at IC21A-2. This will cause a signal flashing at frequency F_2 to appear at IC20A-3 and cause Lamp 8 to flash at the lower frequency and thereby indicate a change in the direction from ON to OFF. Simultaneously, IC19B-13 goes low and causes $\overline{GA}$ to go low. $\overline{CO}$ also goes low.

This change of state is acknowledged by placing a momentary logic 1 at Terminal 19, ARM. This resets IC21A-1 and thereby causes IC20A-3 to go high. Because IC22B-5 is also high, it will cause IC22B-4 to go low and thereby extinguish Lamp 8. This, of course, indicates an OFF, or NO ALARM condition.

The FLASH BUSS input, Terminal P, should be connected to a source of low-frequency squarewaves such as those available from the Model 66 ALRT Alert Card. When a change of state occurs, there will be a logic 0 at Terminal 9, and IC27A-3 will be oscillating at frequency F_1 or F_2, according to the direction of the change.

Lamp common, at Terminals 22 and Z, should have a return path in the external wiring to common at Terminals 1 and A. The wiring should be planned, however, to minimize the effect upon the logic that high surge currents in the lamp-common buss may have.

Whenever a change is detected, Terminal 9, $\overline{CO}$, CHANGE OCCURRED, will be clamped low through a diode such as CR15. Terminal 9's from other 66A LD/CD cards may be connected together to create a $\overline{CO}$ signal buss which will be a logic 0 if any change in any card has occurred. The logic level at this new signal buss will remain low until all the change detectors have been set. This buss should have a single 47K pull-up resistor.

A second buss can be created by wiring together all of the $\overline{GA}$ GENERAL ALARMs at Terminal 15. This buss also requires a 47K pull-up resistor. The buss will be low whenever a change detector is reset, because of the clocking action at the flip-flop corresponding to IC19B. This second buss will stay low until a logic 1 is applied to Terminal 12, ARM GEN ALARM. Form-B contacts may be used instead because of the pull-up action of R20.

In practice, the $\overline{GA}$ buss can be connected to an audible alarm, and the $\overline{CO}$ buss can be wired to a visual display. In this manner, an operator could reset an audible alarm immediately, to prevent annoyance, and yet still have an indication of change.

A logic 1 at LAMP TEST, Terminal 21, will cause all lamps to illuminate, regardless of their status. For this test, IC27A-3 will be at a logic 1 to provide base current into Q2.

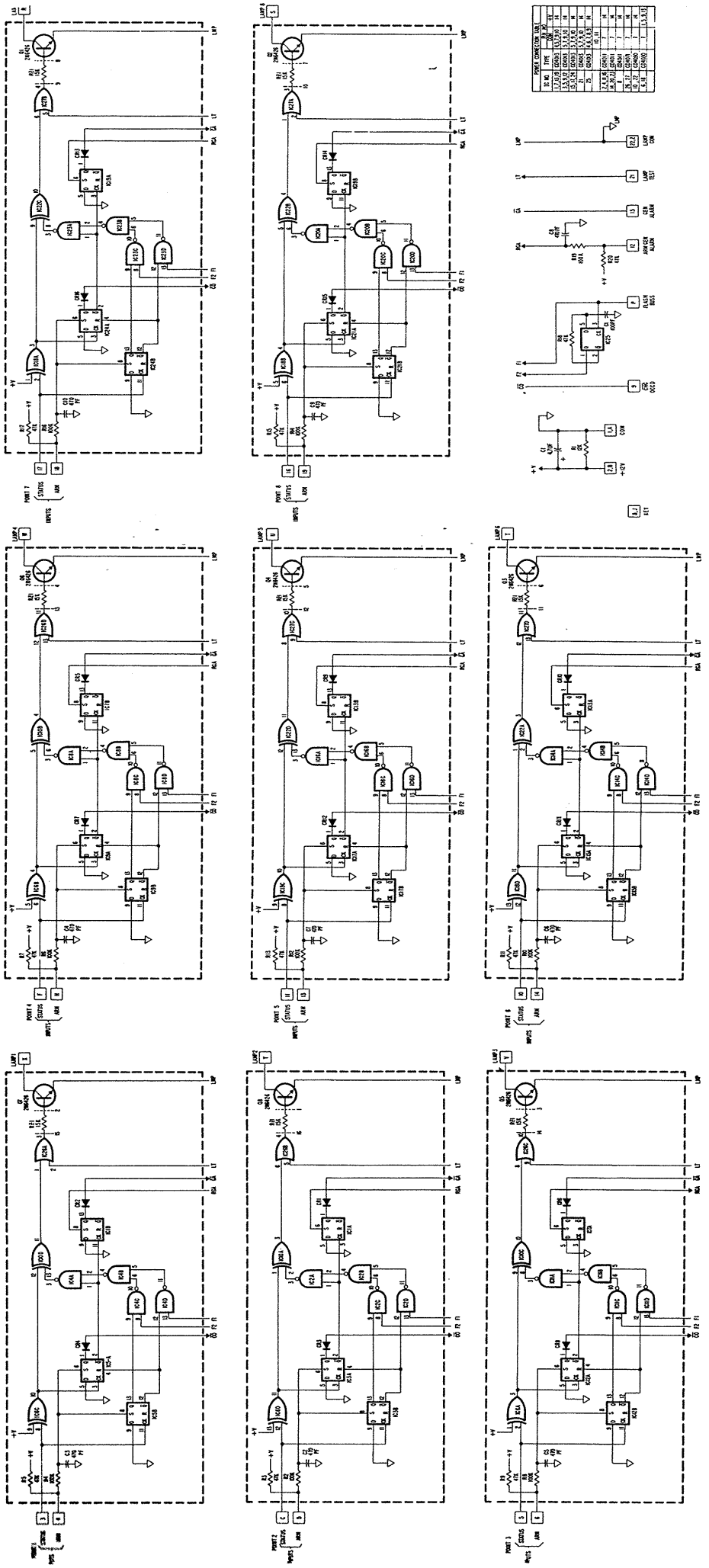

Figure 2. Schematic of circuit, Model 66A LD/CD.

PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	MODEL 66A LD/CD, Assembly HB-44760	
C1	Capacitor, tantalum, 4.7 μF, 20%, 20 V, Kemet T324B475M020AS, or eq.	H-1007-711
C2 thru 10	Capacitor, ceramic, 470 pF, 10%, 100 V, Union Carbide CK12BX471-K, or eq.	H-1007-1358
C11	Capacitor, ceramic, 0.001 μF, 10%, 100 V, Union Carbide CK12BX102K, or eq.	H-1007-1360
CR1 thru 16	Diode, silicon, Type 1N914B/1N4448	HA-26482
IC1, 3, 5, 7, 9, 12, 13, 15, 17, 19, 21, 24, 25	Dual D-type, flip-flop, RCA CD4013AE, or eq.	H-0615-1
IC2, 4, 8, 11, 14, 16, 20, 23	Quad, 2-input NAND gate, RCA CD4011AE, or eq.	H-0615-5
IC6, 10, 18, 22	Quad, EXCL-OR gate, RCA CD4030AR, or eq.	H-0615-22
IC26, 27	Quad, two-input OR gate, RCA CD4071BE, or eq.	H-0615-24
Q1 thru 8	Transistor, Darlington, NPN, Motorola Type 2N6426, or eq.	HA-46531
R1 thru 20	Resistor, fixed, composition, 5%, 1/4W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
RZ1	Resistor, network, 8 ea. 15K, 2%, 1.5w/pkg., Helipot 898-3-R15.0K, or eq.	HA-46704
———	Schematic (Figure 2)	H -44764

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